

## MTech in Integrated Circuits and VLSI Systems

Subject Name	Code	L-T-P	Credit	Contact Hour
<b>Semester-I</b>				
Mathematical Foundations of VLSI Systems	EC6L051	3-0-0	3	3
Analog CMOS VLSI Design	EC6L052	3-1-0	4	4
Digital Integrated Circuit Design	EC6L053	3-1-0	4	4
Elective-I		3-0-0/3-1-0	3/4	3/4
Elective-II		3-0-0/3-1-0	3/4	3/4
Design and Simulation Lab-I	EC6P051	0-0-3	2	3
Semiconductor Devices Lab	EC6P052	0-0-3	2	3
Seminar-I	EC6S051	0-0-3	2	3
<b>Total</b>			<b>23/25</b>	<b>26/28</b>
<b>Semester-II</b>				
CAD for VLSI Design	EC6L054	3-0-0	3	3
VLSI Testing	EC6L055	3-0-0	3	3
Elective-III		3-0-0/3-1-0	3/4	3/4
Elective-IV		3-0-0/3-1-0	3/4	3/4
Elective-V		3-0-0/3-1-0	3/4	3/4
Design and Simulation Lab-II	EC6P053	0-0-3	2	3
Reconfigurable Computing Lab	EC6P054	0-0-3	2	3
Seminar-II	EC6S052	0-0-3	2	3
<b>Total</b>			<b>21/24</b>	<b>24/27</b>
<b>Semester-III</b>				
Thesis Part-I	EC6D051	0-0-0	16	16
Research Review Paper-I	EC6D052	0-0-0	4	4
<b>Total</b>			<b>20</b>	<b>20</b>
<b>Semester-IV</b>				
Thesis Part-II	EC6D053	0-0-0	16	16
Research Review Paper-II	EC6D054	0-0-0	4	4
<b>Total</b>			<b>20</b>	<b>20</b>
<b>Total Credits of the program</b>			<b>84/89</b>	<b>90/96</b>

Subject Name	Code	L-T-P	Credit	Contact Hour
<b>List of Electives (Elective-1 &amp; II)</b>				
Microwave Design and Measurement	EC6L021	3-0-0	3	3
Advanced Digital Signal Processing	EC6L004	3-1-0	4	4
Semiconductor Device Modeling	EC6L017	3-0-0	3	3
Neuromorphic VLSI Hardware	EC6L056	3-0-0	3	3
Advanced Digital System Design	EC6L033	3-1-0	4	4

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List of Electives (Elective-III to V)				
Mixed-Signal VLSI Design	EC6L057	3-0-0	3	3
System-On-Chip Solutions and Architectures Design	EC6L058	3-0-0	3	3
VLSI Physical Design	EC6L059	3-0-0	3	3
Parallel Systems	EC6L060	3-0-0	3	3
IC Design for Wireless Communications	EC6L039	3-0-0	3	3
VLSI Signal Processing	EC6L007	3-0-0	3	3
Architectural Design of VLSI Systems	EC6L061	3-0-0	3	3

### Detailed Syllabus

Subject Name	Code	L-T-P	Credit	Prerequisite
Mathematical Foundations of VLSI Systems	EC6L051	3-0-0	3	None
<p><b>Objective of Course:</b> The objective of this course is to teach fundamentals of numerical optimization processes and some aspects of statistics Applying optimality conditions to formulate circuit design tasks like worst-case and yield analysis and optimization, Differentiated knowledge of circuit sizing tasks, To know what happens inside EDA tools for sizing as a designer, and to be prepared for developing such EDA tools.</p> <p><b>Syllabus:</b> Lagrange function, optimality conditions (constrained, unconstrained); worst-case analysis, classic, realistic, general; multivariate statistical distribution, transformation of distribution functions, expectation values, estimation of expectation values; yield analysis, statistical, geometric, Monte-Carlo analysis; circuit sizing, yield optimization/design centering; structure of an optimization process, univariate optimization, line search, multivariate optimization, polytope method, coordinate search; Newton approach (Quasi-Newton, Levenberg-Marquardt, Least-Squares, Conjugate Gradient; Quadratic Programming (equality/inequality constraints), Sequential Quadratic Programming (SQP); structural analysis of analog circuits, analog sizing rules. Principles of circuit simulation: DC/AC/TR analysis.</p> <p><b>Suggested Text/Reference Books:</b> R. Fletcher, Practical Methods of Optimization, John Wiley &amp; Sons, 2nd Edition, 2000      2000 H. Graeb, Analog Design Centering and Sizing, Springer, 2007.</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
Analog CMOS VLSI Design	EC6L052	3-1-0	4	Electronics/Introduction to Electronics
<p><b>Objective of Course:</b> This course builds the basic concepts and the design of advanced CMOS analog Integrated Circuit. This course focuses on the concepts of MOSFETs and design of amplifiers including non-linear effects. The course will give the practical aspects of CMOS analog IC design. The course aims to teach basic concepts along with advanced design techniques for CMOS amplifiers. The objective of the course is to design and implement the product-level opamps and buffers for VLSI applications.</p>				

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**Syllabus:** Introduction to analog VLSI and mixed signal issues in CMOS technologies; Recapitulation: I-V characteristic of MOS transistors, large signal and small signal models of MOS transistors, device parasitics, feedback configurations and stability theory; Basic MOS models, SPICE models, and frequency dependent parameters; Amplifiers: Basic amplifier topologies and their characteristics, cascode amplifiers, differential amplifier with active load; Biasing circuits: Simple and cascode current mirrors; Two-stage differential amplifier: Analysis for different performance parameters, pole-zero compensation and design, Operational amplifier design, OTA design; Current reference, voltage reference circuits; Comparator: Simple comparator, switch-based comparator, latch-based comparator; Device mismatch and noise analysis.

**Suggested Text/Reference Books:**

Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill Education, Second Edition (2017).  
 Tony Chan Carusone David A. Johns Kenneth W. Martin, Analog Integrated Circuit Design, Wiley, Second Edition (2011)  
 CMOS Analog Circuit Design” by Phillip Allen and Douglas R. Holberg, OUP USA; Third Edition edition (1 September 2011)  
 Operation and Modeling of the MOS Transistor” by Yannis Tsividis, Oxford University, Press; 2 edition, June 26, 2003  
 “Microelectronic Circuits-Theory & Applications” by A.S. Sedra and K.C. Smith, Adapted by A.N. Chandorkar, 6th Edition, Oxford, 2013.

Subject Name	Code	L-T-P	Credit	Prerequisite
Digital Integrated Circuit Design	EC6L053	3-1-0	4	None

**Objective of Course:** CMOS devices and deep sub-micron manufacturing technology. CMOS inverters and complex gates. Modeling of interconnect wires. Optimization of designs with respect to a number of metrics: cost, reliability, performance, and power dissipation. Sequential circuits, timing considerations, and clocking approaches. Design of large system blocks, including arithmetic, interconnect, memories, and programmable logic arrays. Introduction to design methodologies, including laboratory experience. We look at various digital circuit design styles and architectures as well as the issues that designers must face, such as technology scaling and the impact of interconnect. Implementations of basic CMOS logic gates will be discussed first, looking at optimizing the speed, area, or power. The learned techniques will be applied on more evolved designs such as adders and multipliers. The influence of interconnect parasitics on circuit performance and approaches to cope with them are treated in detail. Substantial attention will then be devoted to sequential circuits, clocking approaches and memories. The class includes getting familiar with industrial design automation and verification tools, and using them in assignments, labs and projects.

**Syllabus:** Integration Scales and Applications; Device Modeling for Digital ICs MOSFETs; Layout and fabrication related topics; The Inverter CMOS: DC and transient characteristics; Basic Logic Families; CMOS Logic Circuits; Combinational logic gates; Dynamic circuits and clocking; Digital Logic Units; Sequential design and timing; Arithmetic logic circuits; Memories Cells and Arrays: SRAMs, DRAMs, Applications to Practical Design Problems; Examples from current literature including microprocessors, control systems, and signal processing

**Suggested Text/Reference Books:**

Digital Integrated Circuits 2nd edition, Jan Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Prentice Hall, 2003.  
 Hodges, Jackson, and Selah, Analysis and Design of Digital Integrated Circuits (3rd edition), McGraw-Hill, 2003.  
 S. M. Kang and Y. Leblebici, ‘CMOS Digital Integrated Circuits,’ Tata McGraw Hill, 2003

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Subject Name	Code	L-T-P	Credit	Prerequisite
Design and Simulation Lab-I	EC6P051	0-0-3	2	None
<p><b>Objective of Course:</b> This course is intended to provide hands-on experience on the design of various CMOS analog and RF active and passive circuits, with emphasis on the full design flow up to layout techniques.</p> <p><b>Syllabus:</b> Introduction to IC design tools (Cadence and Mentor Graphics tool); Transistor Characterization; Design of a Common Source, Common Gate and Common Drain Amplifier; Design of a Differential Amplifier; Current-Mirrors; Design of a single and two stage Op-Amps; Design of a BGR; <b>Design of a VCO</b>; Design of a LDO; Introduction to layout techniques; Layout of two-stage Op-amp, Design of RF Integrated Circuits like LNA, Mixer, Power Amplifier, RF and Baseband Filters.</p> <p><b>Suggested Text/Reference Books:</b> Behzad Razavi, Design of Analog CMOS Integrated Circuits McGraw-Hill Education, Second Edition (2017)</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
Semiconductor Devices Lab	EC6P052	0-0-3	2	None
<p><b>Objective of Course:</b> Device Fabrication and Characterization laboratory course will provide a hands-on experience to the fabrication and characterization technology which are used in realization of modern day electronic devices and integrated circuits in the cleanroom environment. The laboratory course will provide an introduction and access to the cleanroom environment, fabrication and analytical equipment, and various processes in the cleanroom. These processes include photolithography, surface patterning, wet and dry-etching, oxygen-plasma etching, structural characterization of the pattern, and metallization. Further, realized pn-junction and photodiode devices will be characterized using probe station. Statistical analysis of the devices from the same batch will also be performed. Following is the detailed course content for this laboratory course</p> <p><b>Syllabus:</b> Introduction to semiconductor manufacturing, wafer production, wafer Identification, wafer handling, wafer cleaning. Introduction to cleanroom, Cleanroom protocols, safety and precautions. Introduction/Recap to various instruments. Visit to the cleanroom and an introduction to various instruments and processes. pn-junction device process, actuators, doping using spin-on dopant photolithography: photoresist, spin-coating, masking, annealing - hands on/demonstration for the same inside the cleanroom. Cleanroom processes such as patterning, oxygen-plasma etching, dry-etching, lift-off, structural characterization of the pattern/actuator: optical characterization, surface profilometer. Metallization of devices using negative photoresist, pattern formation. Device characterization (I-V curve in dark and with illumination), statistical analysis of the devices. Introduction to packaging of the devices.</p> <p><b>Suggested Text/Reference Books:</b> Ghandhi S K, VLSI Fabrication Principles: Silicon and Gallium Arsenide 2nd Edition, Wiley Blackwell (1994) Plummer J D, Deal M D and Griffin P B, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, 1st Edition, Pearson Education (2009) Sze S M, VLSI Technology, 2nd Edition, McGraw Hill Education (2017) Stanley A. Wolf and Richard N. Tauber, Silicon Processing for the VLSI Era Volume 1-Process Technology Lattice Press, 1999 Peter Van Zant, Microchip Fabrication. McGrawHill, 2004</p>				

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Subject Name	Code	L-T-P	Credit	Prerequisite
Microwave Design and Measurement	EC6L021	3-0-0	3	None
<p><b>Objective of Course:</b> This course will be an introduction to microwave circuit design and analysis techniques, with particular emphasis on applications for modern microwave communication and sensing systems. Also, it will cover fundamental measurement techniques for device and circuit characterization at microwave frequencies</p> <p><b>Syllabus:</b> Review of electromagnetics: Maxwell's equations, plane wave solutions. Types of transmission lines and their properties: coaxial lines, rectangular waveguides, Microstrip. Network analysis: scattering matrix, transmission matrix formulations. Matching networks: lumped element designs and limitations, single and double-stub tuned designs, Quarter-wavelength transformers, multisection matching transformers. Active microwave circuit design: characteristics of microwave transistors, mixers and detectors, Oscillators. Amplifier design: LNA and Power amplifiers, gain and stability, design for noise figure. Single-stage amplifier design. Noise in microwave circuits: dynamic range and noise sources, equivalent noise temperature, system noise figure considerations.</p> <p><b>Suggested Text/Reference Books:</b>            David M. Pozar, Microwave Engineering, 3rd. ed., John Wiley &amp; Sons, 2005.            Guillermo Gonzalez, Microwave Transistor Amplifiers, 2nd. ed., Prentice-Hall, 1997.            Thomas H. Lee, Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits, 1st Edition, Cambridge University Press, 2004.</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
Advanced Digital Signal Processing	EC6L004	3-1-0	4	None
<p><b>Syllabus:</b> Multi-rate digital signal processing: decimation, interpolation, sampling rate conversion, digital filter banks, two-channel quadrature mirror filter bank, M-channel QMF bank. Linear prediction and optimum linear filters: forward and backward linear prediction, normal equations, AR lattice and ARMA lattice-ladder filters, Wiener filters, Power spectrum estimation: nonparametric and parametric methods, filter bank methods, Eigen analysis algorithms, Time-frequency analysis: uncertainty principle, Short-time Fourier transform, Wigner distribution, Kernel design, Gabor wavelets, multi-resolution analysis</p> <p><b>Suggested Text/Reference Books:</b>            Digital Signal Processing: Principles, Algorithms and Applications, Proakis and Manolakis, 4th edition, Pearson, 2012            Time-frequency analysis, Cohen, Prentice-Hall, 1995            Advanced digital signal processing, Vaseghi, 4th edition, Wiley, 2008            Multi-rate systems and filter banks, Vaidyanathan, Pearson, 1992</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
Semiconductor Device Modeling	EC6L017	3-0-0	3	NIL
<p><b>Objective of Course:</b> To make the student understand how MOSFET and other semiconductor devices are modeled, impart knowledge to simulate MOSFET for various operational requirements, impart a knowledge on advanced structures of MOSFETs like SOFET, FinFET.</p> <p><b>Syllabus:</b> Review of semiconductor physics: Quantum foundation, Carrier scattering, high field effects; P-N junction diode modeling: Static model, Large signal model and SPICE models; BJT modeling: Ebers - Moll, Static, large-signal, small-signal models. Gummel – Poon model. Temperature and area effects. Power BJT</p>				

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model, SPICE models, Limitations of GP model; Advanced Bipolar models: VBIC, HICUM and MEXTARM; MOS Transistors: LEVEL 1, LEVEL 2, LEVEL 3, BSIM, HISIMVEKV Models, Threshold voltage modeling, Punchthrough, Carrier velocity modeling, Short channel effects, Channel-length modulation, Barrier lowering, Hot carrier effects, Mobility modeling, Model parameters; Analytical and Numerical modeling of BJT and MOS transistors; Types of models for Heterojunction Bipolar Transistors, Compact modeling concepts, Modeling of HBTs, HBT noise models, Measurement and parameter extraction.

### Suggested Text/Reference Books:

S. Karmalkar, NPTEL Video lectures on Solid State Devices and their Transcripts available at: <http://nptel.ac.in/courses/117106091/>

Modules: 0, 1, 7, 9-14 of the following advanced course: S. Karmalkar, NPTEL Video lectures on Semiconductor Device Modeling available at: <http://nptel.ac.in/courses/117106033/>

G. Massobrio, P. Antognetti, Semiconductor Device Modeling with SPICE 2nd edition, McGraw-Hill, New York, 1993.

M Rudolph, Introduction to Modeling HBTs, Artech House, Boston, 2006

S M Sze, K K Ng, Physics of Semiconductor Devices 3rd edition, John Wiley, New Jersey, 2007

G. A. Armstrong, C.K.Maiti, Technology Computer Aided Design for Si, SiGe and GaAs Integrated Circuits IET Series, London, 2007

Nandita Das Gupta, Amitava Das Gupta, "Semiconductor devices, modeling and Technology", Prentice Hall of India, 2004.

Philip.E.Allen Douglas, R. Hoberg, "CMOS Analog circuit Design" Second edition, Oxford Press, 2002.

Subject Name	Code	L-T-P	Credit	Prerequisite
Neuromorphic VLSI Hardware	EC6L056	3-0-0	3	Basic Electronics/Introduction to Electronics

**Objective of Course:** Students will demonstrate the tradeoffs between various neuromorphic implementations starting at a fundamental circuit level through larger system design. Demonstrate analytical modeling of neuromorphic blocks, including the various aspects of computational neuroscience and analog electrical modeling and the relationships between these blocks and will demonstrate utilizing computer design tools and experimental measurement opportunities in the design of neuromorphic architectures, as well as in the design of full analog systems.

**Syllabus:** Introduction to Neuromorphic Engineering; Signalling and operation of Biological neurons, neuron models, signal encoding and statistics; Synapses and plasticity rules, biological neural circuits; Neuromorphic design principles; FETs - device physics and sub-threshold circuits; Analog and digital electronic neuron design; Non-volatile memristive semiconductor devices; Electronic synapse design; Interconnection Networks; Interconnection schemes for large non-spiking and spiking neural networks; Analysis of design, architecture and performance characteristics of demonstrated chips employing Analog neuromorphic VLSI, Digital neuromorphic VLSI, Electronic synapses and other neuromorphic systems. Neuromorphic Systems, Electronic Cochlea, Auditory Localization, Silicon Retinas: Voltage and Current Mode, Neuron Models, Address Event Communication and Motor Pattern Generation.

### Suggested Text/Reference Books:

Shih-Chii Liu, Jörg Kramer, Giacomo Indiveri, Tobias Delbrück, Rodney Douglas, Analog VLSI: circuits and principles, MIT press, 2002, ISBN 0262122553

Carver Mead, Analog VLSI and neural systems, Addison-Wesley, 1989, ISBN0201059924

Eric Kandel, James Schwartz, Thomas Jessell, Steven Siegelbaum, A.J. Hudspeth, Principles of neural science, McGraw Hill 2012, ISBN 0071390111

Dale Purves, Neuroscience, Sinauer, 2008, ISBN 0878936971

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Subject Name	Code	L-T-P	Credit	Prerequisite
Advanced Digital System Design	EC6L033	3-1-0	4	Digital Electronics
<p><b>Objective of Course:</b> This course introduces the students to state-of-the-art design methodologies through practical design applications. Students will learn and design complete systems with FPGAs that includes coding, testing, synthesizing and implementation. In this process, students will also learn the best coding practices, and optimize the design for performance, area, and power. The main objective of the course is “Learn by doing rather than just reading”. Students will also get a chance to try and experiment a lot through the assignments and term project.</p> <p><b>Syllabus:</b> Advanced topics in combinational and sequential design: Use of CAD, design methodologies, system decomposition, arithmetic modules, and design of complex sequential systems. Introduction to FPGA architectures: Overview, programming technologies, configurable logic block, FPGA routing architectures. Logic design with Verilog: Introduction to Verilog, logic design with behavioral models of combinational and sequential logic, synthesis of combinational and sequential logic, design and synthesis of data path controllers, programmable logic and storage devices, algorithms and architectures for digital processors, architectures for arithmetic processors, coding for FPGAs. Designing with FPGAs: Design flow for FPGAs, prototyping with FPGAs, and debugging. (Utilize commercial FPGA development tools for compilation, simulation, synthesis, implementation, and debugging).</p> <p><b>Suggested Text/Reference Books:</b></p> <p>Advanced Digital Design with the Verilog HDL (2nd Edition 2017) by Michael D.Ciletti. 2017            Verilog HDL (2nd Edition) by Samir Palnitkar. ISBN: 9788177589184, Publisher: Pearson, 2003            Digital System Design with FPGA: Implementation Using Verilog and VHDL by Cem Unsalan, Bora Tar, ISBN: 9781259837906, McGrawHill Publications. 2015            Designing with Xilinx FPGAs using Vivado, Editor, Sanjay Churiwala, Springer 2016.            Advanced FPGA Design: Architecture, Implementation, and Optimization by Steve Kilts. ISBN: 9780470054376, Publishers: Wiley, 2007            Field-Programmable Gate Arrays: Reconfigurable Logic for Rapid Prototyping and Implementation of Digital Systems by Richard C. Dorf, John V. Oldfield. ISBN: 9788126516612, Publisher: Wiley, 2008</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
CAD for VLSI Design	EC6L054	3-0-0	3	Digital Electronics
<p><b>Objective of Course:</b> At the end of the module students are expected to be capable of employing algorithms for computer-aided design of (digital) integrated circuits, electronic systems, and other emerging platforms. These comprise: synthesis and optimization of digital circuits on logic level; simulation of digital circuits on logic level; mixed integer linear programming (MILP) modeling of EDA problems. With a good understanding of the inner workings of modern EDA tools, students can use and develop EDA tools more effectively and efficiently</p> <p><b>Syllabus:</b> Introduction to Semiconductors and Design Flow, Representation of digital circuits by Boolean functions, Optimization of combinatorial two-level digital circuits: Quine-McCluskey; Karnaugh diagram; cube graph; resolution method; combinatorial optimization (cofactor, Boole’s expansion); BDDs. Optimization of multi-level, multi-output, incompletely specified Boolean functions: Sharing of logic; finding common cubes; utilizing “don’t cares”; functional decomposition. Optimization of sequential</p>				

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circuits: Representation of sequential circuits by FSMs; optimization of FSMs; binary coding of FSMs. Fundamental introduction to digital simulation concepts and Verilog. Testing of digital circuits: Introduction to testing; Fault tables; Boolean difference; structure-oriented computation of Boolean difference; fault simulation; fault trees; D-Algorithm; testing of sequential circuits; Design for testability. Mixed Integer Linear Programming (MILP) Modeling: properties of modeling method, mathematical modeling techniques (constraint linearization, OR-relation transformation, propositional logic modeling, absolute value modeling), modeling common EDA problems including grid routing, gridless routing, escape routing on printed circuit board (PCB), area routing on PCB, non-overlapping placement, area minimization, network flow, etc.

### Suggested Text/Reference Books:

Algorithms for VLSI Design Automation; Sabih H. Gerez; John Wiley & Sons,1999  
 Synthesis and Optimization of Digital Circuits; De Micheli, Giovanni; McGraw-Hill,1994  
 VLSI Physical Design Automation; S. Sait, H. Youssef; McGraw-Hill, 1995  
 Applied Mathematical Programming; Bradley, Hax, and Magnanti; Addison-Wesley, 1977

Subject Name	Code	L-T-P	Credit	Prerequisite
VLSI Testing	EC6L055	3-0-0	3	None
<p><b>Objective of Course:</b> Testing is an integral part of the VLSI design cycle. With the advancement in IC technology, designs are becoming more and more complex, making their testing challenging. Testing occupies 60-80% time of the design process. A well structured method for testing needs to be followed to ensure high yield and proper detection of faulty chips after manufacturing. Design for testability (DFT) is a matured domain now, and thus needs to be followed by all the VLSI designers. In this context, the course attempts to expose the students and practitioners to the most recent, yet fundamental, VLSI test principles and DFT architectures in an effort to help them design better quality products that can be reliably manufactured in large quantity.</p> <p><b>Syllabus:</b> Physical faults and their modeling. Fault equivalence and dominance; fault collapsing. Fault simulation: parallel, deductive and concurrent techniques; critical path tracing. Test generation for combinational circuits: Boolean difference, D-algorithm, PODEM, etc. Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage.</p> <p><b>Suggested Text/Reference Books:</b>                      M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing", Kluwer Academic Publishers, 2000                      N.K. Jha and S. Gupta, "Testing of Digital Systems", Cambridge University Press 2004                      M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems Testing and Testable Design", Wiley-IEEE Press,1993                      P.H. Bardell, W.H. McAnney and J. Savir, "Built-in Test for VLSI: Pseudorandom Techniques", Wiley Interscience, 1987                      L-T. Wang, C-W. Wu and X. Wen, "VLSI Test Principles and Architectures", Morgan Kaufman Publishers, 2006                      P.K. Lala, "Fault Tolerant and Fault Testable Hardware Design", Prentice-Hall Intl 1985</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
Design and Simulation Lab-II	EC6P053	0-0-3	2	None
<p><b>Objective of Course:</b> This course is intended to provide hands-on experience on the design of various CMOS digital circuits, and hardware description languages with emphasis on the full design flow.</p>				



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**Syllabus:** Introduction to digital circuit simulators– NGSPICE and Cadence tools for circuit and layout simulations; SPICE models of CMOS devices; Static and dynamic characterization of CMOS inverters, gate delay and interconnect delay in CMOS; Combinational and sequential static CMOS circuits including pass transistors; Dynamic CMOS logic circuits; Introduction to hardware description languages (VHDL/Verilog)- analysis, elaboration, and synthesis of HDLs and implementation on FPGAs.

**Suggested Text/Reference Books:**

S. M. Kang and Y. Leblebici, `CMOS Digital Integrated Circuits' Tata McGraw-Hill

Subject Name	Code	L-T-P	Credit	Prerequisite
Reconfigurable Computing Lab	EC6P054	0-0-3	2	None

**Objective of Course:**

The purpose of this lab “reconfigurable computing” is to instruct students about the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques by providing them the necessary knowledge for understanding and designing reconfigurable hardware systems and studying applications benefiting from dynamic hardware reconfiguration.

**Syllabus:** Introduction to XILINX FPGA families, Vivado Design Flow, and various FPGA boards, Implementation of combinational circuits such as full adders, subtractors, multiplexers, decoders, comparators. Implementation of sequential elements such as latches, flip-flops, and circuits like counters, shift registers, and sequence detectors. Desig of data path and control paths and prototyping. Introduction to ZYNQ FPGAs, integration of ARM proesors using AHB bus, and control/configuration of FPGA using ARM core. Introduction to Vivado HLS flow and implementation of simple algorithms/designs. Introduction to PYNQ boards and implementation of simple algorithms/designs.

**Suggested Text/Reference Books:**

Digital System Design with FPGA: Implementation Using Verilog and VHDL, TMH 2017

Designing with Xilinx FPGAs: Using Vivado, 2016

Subject Name	Code	L-T-P	Credit	Prerequisite
Mixed-Signal VLSI Design	EC6L057	3-0-0	3	None

**Objective of Course:** Focuses on analog-to-digital and digital-to-analog converters in bipolar and CMOS technologies. Course content includes discussions of applications, appropriate system specifications, circuit elements, topology tradeoffs, and history.

**Syllabus:** Sampling theory and discrete-time signals; sample-and-hold circuits; Switch design and switched capacitor circuits; Comparators; Basics of data converters; quantization, ADC and DAC metrics; Nyquist rate ADC's: SAR and pipelines ADC's; Nyquist rate DACs's; Architectures and design of Nyquist rate DAC's; High-resolution data converters (sigma-delta data converters); Mixed-signal layout design; Integrated power management units (Bulk Converter and LDO); Selected topics in mixed-signal VLSI circuits

**Suggested Text/Reference Books:**

1 Data Conversion System Design, by B. Razavi, IEEE Press, 1995

2 Tony Chan Carusone David A. Johns Kenneth W. Martin, Analog Integrated Circuit Design, Wiley, Second Edition 2011

3. Understanding Delta-Sigma Data Converters, by R. Schreier and G.C. Temes, IEEE Press/Wiley, 2004

4. Data Converters, F. Maloberti, Springer, 2007

5. Analog-to-Digital Conversion, M. Pelgrom, second ed., Springer, 2013

6. Journals and Conferences papers from IEEE SSCS, and IEEE CAS Societies.

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System-On-Chip Solutions and Architectures Design	EC6L058	3-0-0	3	Digital Electronics
<p><b>Objective of Course:</b> The objective of this course is to impart a general understanding of the structure and operation of systems-on-chip. Main building blocks of a system-on-chip, e.g., processor, on-/off-chip memories, interconnect is introduced. Implementation methods as well as techniques for low power consumption are addressed.</p> <p><b>Syllabus:</b> This course provides basics, current trends and challenges in the development of digital system-on-chip (SoC). We start with the main steps for building arbitrary CMOS-based combinatorial logic and sequential digital data processing and control circuitry (e.g. Finite State Machines) and explaining their role and significance in the scope of key system-on-chip components: microprocessors, memories and interconnects. The microarchitectural structure and building blocks of processor elements (RISC cores), on-/off-chip memory technology (SRAM, DRAM, Flash), bus and point-to-point interconnect standards (Processor Local Bus, Advanced Microcontroller Bus Architecture, FIFO) as well as the design of communications specific arithmetic blocks (adder, multipliers, shift and comparators) will be introduced and analyzed. Finally, we will introduce main implementation methods for SoCs, such as FPGA, standard cell and full custom design, and discuss methods for low power design, which is vital for the development of SoCs in embedded systems.</p> <p><b>Suggested Text/Reference Books:</b>            J. Hennessy, "Computer Architecture. A Quantitative Approach", Elsevier            J. Rabaey, "Digital Integrated Circuits", Prentice Hall            N. Weste, K. Eshraghian, "Principles of CMOS VLSI Design", Addison Wesley</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
VLSI Physical Design	EC6L059	3-0-0	3	None
<p><b>Objective of Course:</b> The course will introduce the participants to the basic design flow in VLSI physical design automation, the basic data structures and algorithms used for implementing the same. The course will also provide examples and assignments to help the participants to understand the concepts involved, and appreciate the main challenges therein. At the end of the course, the students will be able to a) analyze different algorithms for partition, b) analyze to place and partition the blocks while for designing the layout for IC, c) solve the performance issues in circuit layout, d) analyze the problem formulations for clock-tree routing, and e) analyze the timing and performance constraints.</p> <p><b>Syllabus:</b> Introduction to physical design automation. Partitioning, Floorplanning and Placement. Grid Routing and Global Routing, Detailed Routing and Clock Design. Clock Routing and Power/Ground. Static Timing Analysis and Timing Closure. Physical Synthesis and Performance Driven Design Flow: Interconnect Modeling and Layout Compaction. Introduction to Testing, Fault Modeling and Simulation. Test Pattern Generation, DFT and BIST. Low Power Design Techniques.</p> <p><b>Suggested Text/Reference Books:</b>            Andrew B. Kahng, Jens Lienig, Igor L. Markov and Jin Hu "VLSI Physical Design: From Graph Partitioning to Timing Closure". 2011            Naveed A. Sherwani "Algorithm for VLSI Physical Design Automation", 3rd Edition, Springer, 1998            Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer, 2008</p>				

## MTech in Integrated Circuits and VLSI Systems

Subject Name	Code	L-T-P	Credit	Prerequisite
Parallel Systems	EC6L060	3-0-0	3	NIL
<p><b>Objective of Course:</b> Modern PCs allow parallel execution of tasks. The efficient use of this parallelism however needs more than only multiple processor cores. The problem itself must be parallelisable. In this course characteristics of different parallel architectures and metrics of evaluation are described. Furthermore, models and languages for programming parallel computers are shown.</p> <p><b>Syllabus:</b> Theory of parallelism (parallel computer models, parallel specification forms and languages, performance models and calculation). Classification of parallel and scalable computer architectures (multiprocessors and multicomputers, vector computers, data flow machines, VLSI computing fields) Programmable System-on-Chip (SoC) architectures Programming of parallel computers (languages and models, design methods and compilers, optimization) Massive Parallelism: From Algorithm to Circuit Theoretical and practical exercises with computer-aided tools deepen the knowledge.</p> <p><b>Suggested Text/Reference Books:</b>                      Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability"                      Michael Wolfe, "High Performance Compilers for Parallel Computing"                      Alain Darte, Yves P. Robert, Frederic Vivien, "Scheduling and Automatic Parallelization"                      Utpal Banerjee, "Loop Parallelization (VLSI, Computer Architecture and Digital Signal Processing)"                      S. Y Kung, "VLSI Array Processors"</p>				

Subject Name	Code	L-T-P	Credit	Prerequisite
IC Design for Wireless Communications	EC6L039	3-0-0	3	Analog IC Design
<p><b>Objective of Course:</b> Modern integrated wireless communication systems have fundamentally changed the way we live our everyday life, and they will become even more important in the future. Extensive research is underway in the next generation wireless communication systems such as in spectrum sharing, 5G radios, radios for the internet-of- things (IoT's) and millimetre wave transceivers for communication and sensing with the help of scaled CMOS technology. The goal of this course is to convey a methodical design approach for the design of Integrated Circuits for Wireless Communications. The course introduces the principles, analysis, and design of CMOS radio frequency integrated circuits (RFIC) for wireless communication systems. Besides system level design considerations for RF IC, this course also provides the rule-of-thumb approach in designing main RF blocks. A part of the course consists of term projects using modern VLSI design software and foundry RF models.</p> <p><b>Syllabus:</b>                      Introduction to wireless/RF CMOS IC Design: Acronyms, Applications, RF viewpoints, definitions and wireless specifications. System Architecture for Wireless Transceivers: Super-heterodyne, homodyne/direct-conversion, sliding-IF architectures etc., Wireless Communication Standards: WLAN, IoT, LTE, 5G, 5G-NR, Bluetooth, I-IoT, NB-IoT etc., Low-Noise Amplifiers: LNA Trade-offs, design requirements, different circuit topologies, matching, inductors design. Mixers: up-conversion and down-conversion mixers, mixer fundamentals and characterization, image rejection, up-conversion and down-conversion mixer circuit topologies, phase-shifters, sampling mixers, subsampling mixers. Introduction to Power Amplifiers: design requirement, approaches, circuit topologies, digital direct synthesis, examples. Clocking Circuits: Oscillators, phase-locked loops, Frequency Synthesizers- Introduction to Fractional-N and Integer-N frequency synthesizers, Study of few complete single-chip RF transceivers, system-to-circuit design examples for a reference wireless standard.</p>				

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### Suggested Text/Reference Books:

B. Razavi, RF Microelectronics, 2e Paperback – 1 January 2013, Pearson Education India; 2nd edition (1 January 2013), ISBN-13: 978-9332518636.

Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press; 2nd edition (22 December 2003).

Latest articles from the IEEE Journal of Solid-State Circuits, IEEE Transactions on Circuits and Systems-I and II, IEEE Transactions on Microwave Theory and Techniques.

Conference proceedings of IEEE ISSCC, ESSCIRC, RF IC Design, CICC etc.,

Gu, Qizheng, RF System Design of Transceivers for Wireless Communications, Springer, 2005, ISBN 978-0-387-24162-3

Gabriele Manganaro and Domine Leenaerts, Advances in Analog and RF IC Design for Wireless Communication Systems, 2013, Elsevier Inc., ISBN 978-0-12-398326-8

Subject Name	Code	L-T-P	Credit	Prerequisite
VLSI Signal Processing	EC6L007	3-0-0	3	None

**Objective of Course:** This course will cover the most important methodologies for designing custom or semi-custom VLSI systems for some typical digital signal processing applications. Students will get to learn, how to map DSP algorithms into VLSI efficiently. Several high-level algorithm and architecture design techniques will be introduced that enable joint optimization across the algorithmic, architectural, and circuit domains. General techniques covered include pipelining, retiming, folding and unfolding, and systolic array design. Mapping of algorithms on array structures, DSP systems, and Field Programmable Gate Arrays (FPGAs) will be described for selected algorithms.

**Syllabus: Introduction:** Typical signal processing algorithms, overview of VLSI architectures, representations of DSP algorithms. General techniques: Iteration bound, pipelining, parallel processing, and computer arithmetic. Retiming techniques: Definitions, general methodology, retiming for critical path reduction. Unfolding and folding techniques: Unfolding algorithm, critical path, unfolding, and retiming, folding transformation, register minimization. Systolic Architectures: Overview, design methodology, matrix operations and 2D systolic array design. Mapping Algorithms onto Array Structures: Parallel algorithm expressions, canonical mapping methodology, generalized mapping. Programmable Signal Processors: Important features, FFT architectures, DSP processors for mobile and wireless communications, processors for multidimensional signal processing. Reconfigurable DSP Architectures: DSP design using VLIW architectures, PACT-XPP, Tightly-Coupled Processor Arrays, etc., advanced multimedia applications.

### Suggested Text/Reference Books:

Keshab K.Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation" John Wiley, Indian Reprint, 2007

Architectures for Digital Signal Processing Paperback by Peter Pirsch John Wiley, 2009

U. Meyer-Baese, Digital Signal Processing with Field Programmable Arrays Springer, Second Edition, Indian Reprint, 2007

VLSI array processors by Sun Yuan Kung Prentice Hall, 1998

VLSI Design Methodologies for Digital Signal Processing Architectures by Magdy A. Bayoumi Springer 1994

Sanjit K. Mitra, Digital Signal Processing: A computer based Approach TMH, 2006

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Subject Name	Code	L-T-P	Credit	Prerequisite
Architectural Design of VLSI Systems	EC6L061	3-0-0	3	None
<p><b>Objective of Course:</b> The course provides an essential background to the architectural design of VLSI, VLSI Design flow, and general design methodologies. It will cover different aspects of signal flow, timing analysis and hierarchical system design. It will also cover building blocks of VLSI design in details and also different architectures.</p> <p><b>Syllabus:</b> VLSI Design flow, general design methodologies; Mapping algorithms into Architectures: Signal flow graph, data dependences, datapath synthesis, control structures, critical path and worst case timing analysis, concept of hierarchical system design; Datapath elements: Datapath design philosophies, fast adder, multiplier, driver etc., datapath optimization, application specific combinatorial and sequential circuit design, CORDIC unit; Pipeline and parallel architectures: Architecture for real time systems, latency and throughput related issues, clocking strategy, power conscious structures, array architectures; Control strategies: Hardware implementation of various control structures, microprogrammed control techniques, VLIW architecture; Testable architecture: Controllability and observability, boundary scan and other such techniques, identifying fault locations, self reconfigurable fault tolerant structures; Tradeoff issues: Optimization with regard to speed, area and power, asynchronous and low power system design, ASIC (application specific integrated circuits) and ASISP (application specific instruction set processors) design;</p> <p><b>Suggested Text/Reference Books:</b> Computer Arithmetic: Algorithms and Hardware Designs by B. Parhami 2000 Digital Arithmetic (M. D. Ercegovac and T. Lang) 2004 Advanced Arithmetic for the Digital Computer (K. Ulrich)2002</p>				